सत्यमेव जयते

INTELLECTUAL PROPERTY **INDIA**

GOVERNMENT OF INDIA
MINISTRY OF COMMERCE & INDUSTRY,
PATENT OFFICE, DELHI BRANCH,
W - 5, WEST PATEL NAGAR,
NEW DELHI - 110 008.

I, the undersigned being an officer duly authorized in accordance with the provision of the Patent Act, 1970 hereby certify that annexed hereto is the true copy of the ***Application, Complete Specification*** *and* ***Drawing Sheets*** *filed in connection with Application for Patent No.**1237/Del/2002** dated **10th December 2002.***

Witness my hand this 22nd day of December2003.

(S.K. PANGASA)
Assistant Controller of Patents & Designs

1237-2

FORM 1

THE PATENTS ACT, 1970

(39 of 1970)

APPLICATION FOR GRANT OF A PATENT

(See Sections 5(2), 7, 54 and 135)

1 3 DEC 2002

1. I/we,

STMicroelectronics Pvt. Ltd., an Indian company, of Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India.

2. hereby declare –

(a) that I am/we are in possession of an invention titled *"Integrated Low Dropout Linear Voltage Regulator With Improved Current Limiting."*

(b) that the ~~provisional~~ / complete specification relating to this invention is filed with this application

(c) that there is no lawful ground of objection to the grant of a patent to me/us.

3. further declare that the inventor(s) for the said inventions is/are

(i) BANSAL Nitin, an Indian national, of 6/115, Shivaji Nagar, Gurgaon – 122001, Haryana.

4. I/we claim the priority from the application(s) filed in convection countries, particulars of which are as follows: **NA**

5. I/we state that the said invention is an improvement in or modification of the invention the particulars of which are as follows and of which I/we are the applicant/patentee: **NIL**

6. I/we state that the application is divided out of my/our application, the particulars of which are given below and pray that this application be deemed to have been filed on under section 16 of the Act. **NIL**

7. That I am/we are the assignee or legal representative of the true and first inventors.

8. That my/our address for service in India is as follows:

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PUBLICATION

02-IND-072

Form 2

1237-2

THE PATENTS ACT, 1970

10 DEC 2002

COMPLETE SPECIFICATION

[See Section 10]

'INTEGRATED LOW DROPOUT LINEAR VOLTAGE REGULATOR WITH IMPROVED CURRENT LIMITING'

STMicroelectronics Pvt. Ltd., *Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 301, Uttar Pradesh, India, an Indian Company*

The following specification particularly describes and ascertains the nature of this invention and the manner in which it is to be performed.

from the drawback that the sense resistor causes a voltage drop leading to an undesired increase in voltage dropout.

US Patent 4,254,372 describes a current sensing method for Low Dropout regulators. In this method, instead of inserting a resistor in the output path, a sense resistance is inserted in the path of the base current drive of the PNP series pass transistor. The base current is sensed through the sense resistance and is used to control the output current by limiting the base current to a predetermined value corresponding to a maximum allowable load current. However, this arrangement can only be used when the output pass transistor is a Bipolar Junction Transistor (BJT). Modern integrated circuits based on Metal Oxide Semiconductor (MOS) transistors cannot therefore utilize this technique. The technique is also not very convenient for BJT applications owing to the wide variation in current gain between individual series pass transistors.

Object and Summary of the Invention

The object of the invention is to obviate the above disadvantages and provide an LDO linear voltage regulator with improved current limiting.

Another object of this invention is to provide an improved current limiting mechanism that is usable for both MOS and BJT implementations

To achieve the said objectives this invention provide an integrated Low Dropout (LDO) linear voltage regulator providing improved current limiting, comprising:

- a 2-input, 1-output difference voltage amplifier consisting of a differential pair ,
- a reference voltage source connected to a first input of the difference voltage amplifier,
- an arrangement to sense the output voltage of the voltage regulator and couple it to the second input of the difference amplifier in a manner that provides negative feedback,
- a series pass transistor connected to the output of the difference voltage amplifier,
- a current sense transistor coupled to the series pass transistor using current mirroring to monitor the current passing through it,

- coupling the junction of the current sense transistor and the reference current source to the difference voltage amplifier in a manner that increases the apparently sensed voltage as the current through the current sense transistor exceeds the reference current value.

The arrangement for sensing the output voltage of the voltage regulator consists of directly connecting the output of the voltage regulator to the second input of the difference amplifier.

Brief Description of the Drawings:

The invention will now be described with reference to the accompanying drawings.

Figure 1 shows a schematic block diagram of the prior art circuit for LDO.

Figure 2 shows a schematic circuit diagram of the LDO linear voltage regulator with improved current limiting in accordance with the present invention.

Figure 3 shows waveforms defining the operation of the current limiter in a LDO linear voltage regulator according to the present invention.

Detailed Description:

Figure 1 has already been described in the background to the invention.

Fig.-2 shows a preferred embodiment of the improved LDO linear voltage regulator according to this invention. This embodiment is merely illustrative and is not intended to be limiting in any manner. For instance, the embodiment shows a Complementary Metal Oxide Semiconductor (CMOS) implementation, however a Bipolar (BJT) implementation is equally possible. Similarly, the embodiment shows a unity gain configuration for the regulator, though non-unity gain configurations are equally feasible. Referring to **figure 2,** the improved LDO voltage regulator includes a differential amplifier **10** and an output stage incorporating current sensing and current limiting circuitry comprising two branches of pass transistors, each branch comprising a pair of complementary transistors **M6, M7,** and **M8, M9**. The pass transistor **M6** which is in one branch and the corresponding current sense transistor **M8** in the other branch have their control terminals (gates) connected together at vg, and their Source terminals connected together at the common supply terminal. Since both transistors are located on the same silicon die, are fabricated with the same process, are sized proportionately and are (preferably) located in close proximity to each other, this

The circuit operation can be understood from **figure 3.** In general the output ***vo*** sits at the same voltage level as ***vref*** because of negative feedback and voltage follower configuration used. When higher current is drawn from the load at the output ***vo*** tends to decrease as shown in **figure 3a**. As ***vo*** is connected to the control terminal of the pass transistor **M1**, the decrease in ***vo*** causes the gate overdrive voltage of **M1** to decrease. This reduced overdrive voltage of **M1** results in decrease of current through pass transistor **M1**. According to differential amplifier characteristics, a decrease in current of branch **B1** results in a corresponding increasing in current in branch **B2** thus lowering of ***vg***. The decrease in ***vg*** increases the gate overdrive voltage of pass transistor **M6** enabling it to provide higher current without appreciable fall in ***vo***.

The output voltage ***vo*** and corresponding current through transistor **M1** is allowed to decrease on demand of the higher output current until the output current reaches a desired/critical pre-decided current value which is set by the reference current flowing through M9. The reference current value can be set by properly sizing transistors in the current sensing and limiting branch of circuit. The pass transistor **M8** whose size is proportional to **M6** gives a current proportional to the load current.. The current limit is determined by the empirical relation :

$$\frac{I_{out}}{I_s} = \frac{W_{M6}}{W_{M8}}$$

i.e. $$\frac{600mA}{Is} = \frac{27000um}{40um}$$

i.e. $$Is \sim 900uA$$

This would mean that **M9** should be set for a reference current of 900uA for a current limit of 600 mA.

If the current in the pass transistor **M8** is less than reference current ***vs*** remains near zero. Thus during the normal operation of the regulator when the load current being drawn is less than the set current limit the transistor **M10** would not be operational and the differential amplifier acts purely as an error amplifier. When the current in pass transistor **M6** becomes

We claim:

1. An integrated Low Dropout (LDO) linear voltage regulator providing improved current limiting, comprising:
   - a 2-input, 1-output difference voltage amplifier consisting of a differential pair ,
   - a reference voltage source connected to a first input of the difference voltage amplifier,
   - an arrangement to sense the output voltage of the voltage regulator and couple it to the second input of the difference amplifier in a manner that provides negative feedback,
   - a series pass transistor connected to the output of the difference voltage amplifier,
   - a current sense transistor coupled to the series pass transistor using current mirroring to monitor the current passing through it,
   - a reference current source coupled to the output of the current sense transistor, and
   - the junction of the current sense transistor and the reference current source being connected to the difference voltage amplifier in a manner that increases the apparently sensed voltage as the current through the current sense transistor exceeds the reference current value.

2. An integrated Low Dropout (LDO) linear voltage regulator as claimed in claim 1, wherein the difference voltage amplifier is a long-tailed pair having a constant current source for providing the tail current.

3. An integrated Low Dropout (LDO) linear voltage regulator as claimed in claim 1, wherein the arrangement for sensing the output voltage of the voltage regulator consists of directly connecting the output of the voltage regulator to the second input of the difference amplifier.

4. An integrated Low Dropout (LDO) linear voltage regulator as claimed in claim 2, wherein the junction of the current sense transistor and the reference current source is connected to the control terminal of a current limiting transistor that is connected in

8. A method for improving current limiting in an integrated low Drop Out (LDO) linear voltage regulator substantially as herein described with reference to and as illustrated in Figure 2 and 3 of the accompanying drawings.

Dated this 10th day of December 2002

Shanti Kumar

of **ANAND & ANAND, Advocates**
Agents for the applicants

ABSTRACT

This invention relates to an integrated Low Dropout (LDO) linear voltage regulator providing improved current limiting, comprising a 2-input, 1-output difference voltage amplifier consisting of a differential pair and a reference voltage source connected to a first input of the difference voltage amplifier. The invention also includes an arrangement to sense the output voltage of the voltage regulator and couple it to the second input of the difference amplifier in a manner that provides negative feedback, a series pass transistor connected to the output of the difference voltage amplifier. A current sense transistor is coupled to the series pass transistor using current mirroring to monitor the current passing through it. A reference current source is coupled to the output of the current sense transistor, and the junction of the current sense transistor and the reference current source are connected to the difference voltage amplifier in a manner that increases the apparently sensed voltage as the current through the current sense transistor exceeds the reference current value.

The invention also provides a method for improving current limiting in an integrated low Drop Out (LDO) linear voltage regulator.

Prior Art

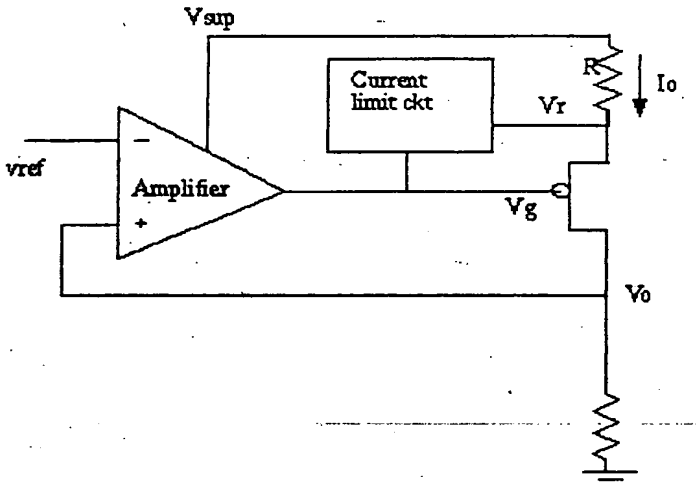

Fig. 1

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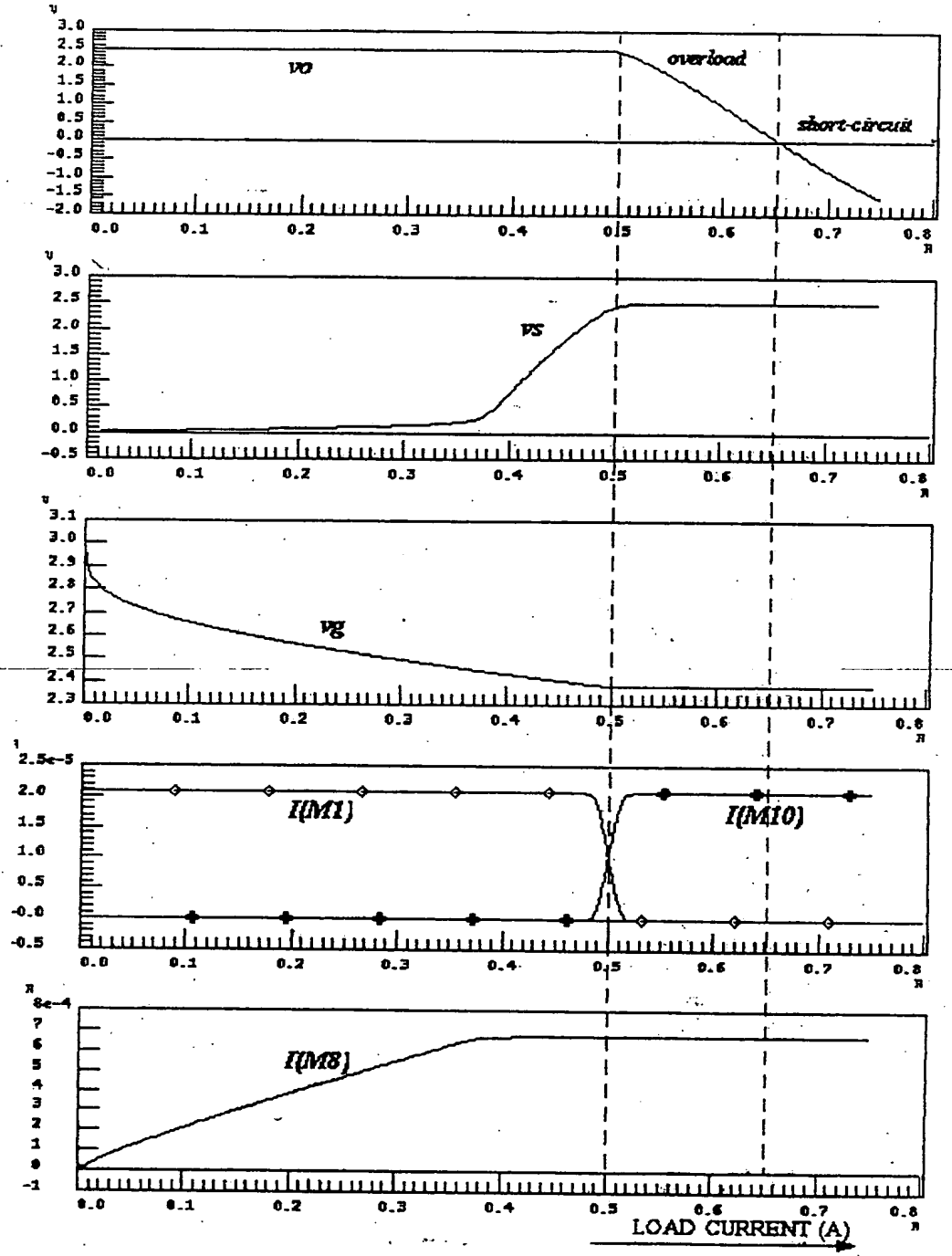

Fig. 3

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